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PATENT & TRADEMARK OFFICE

2

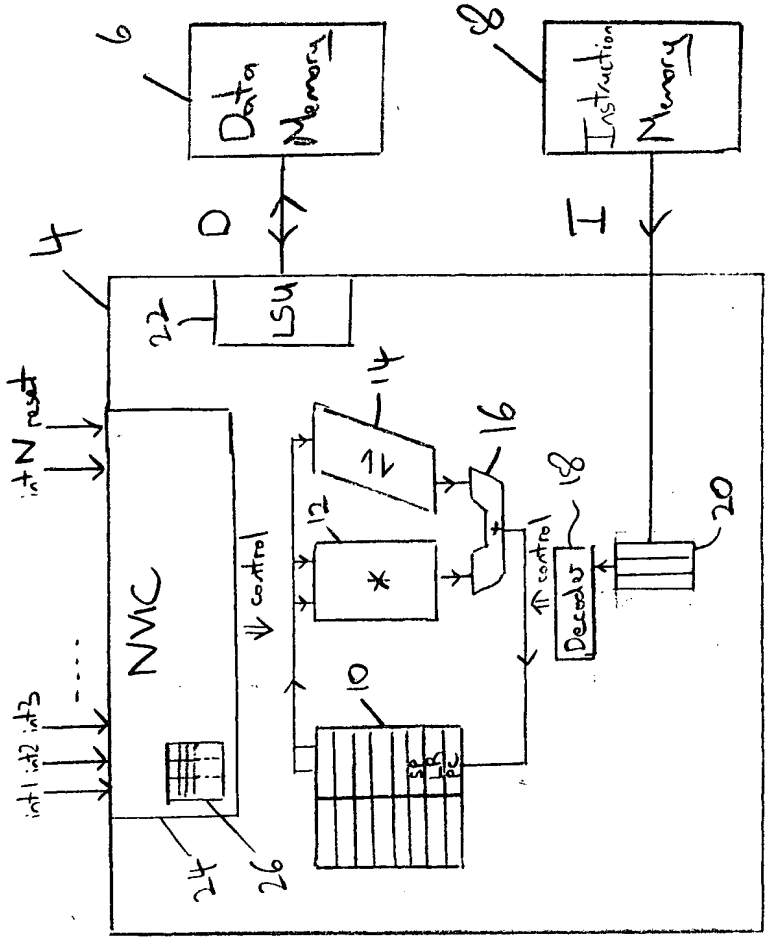

Fig 1

NVIC Control Table

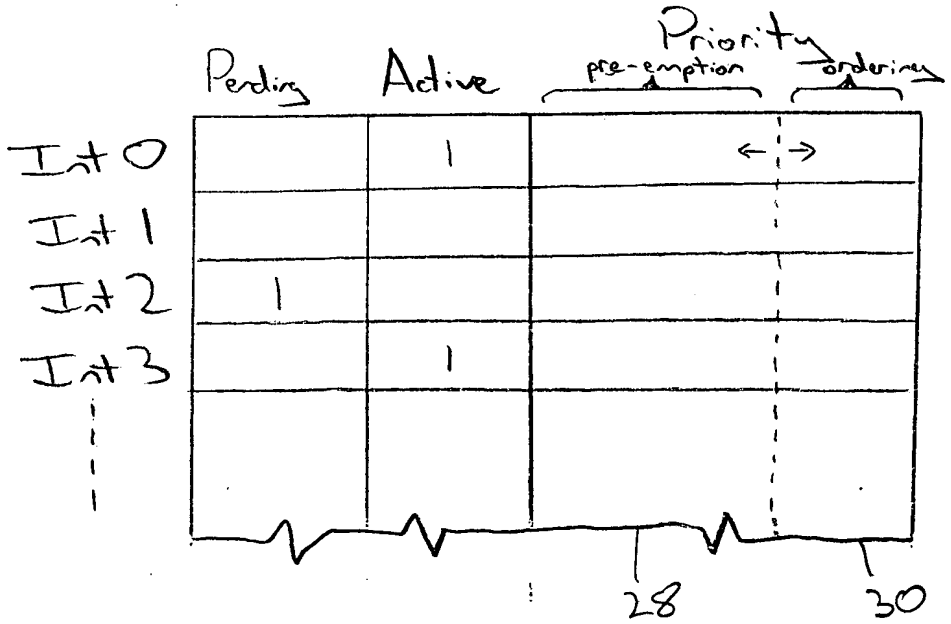

Fig. 2

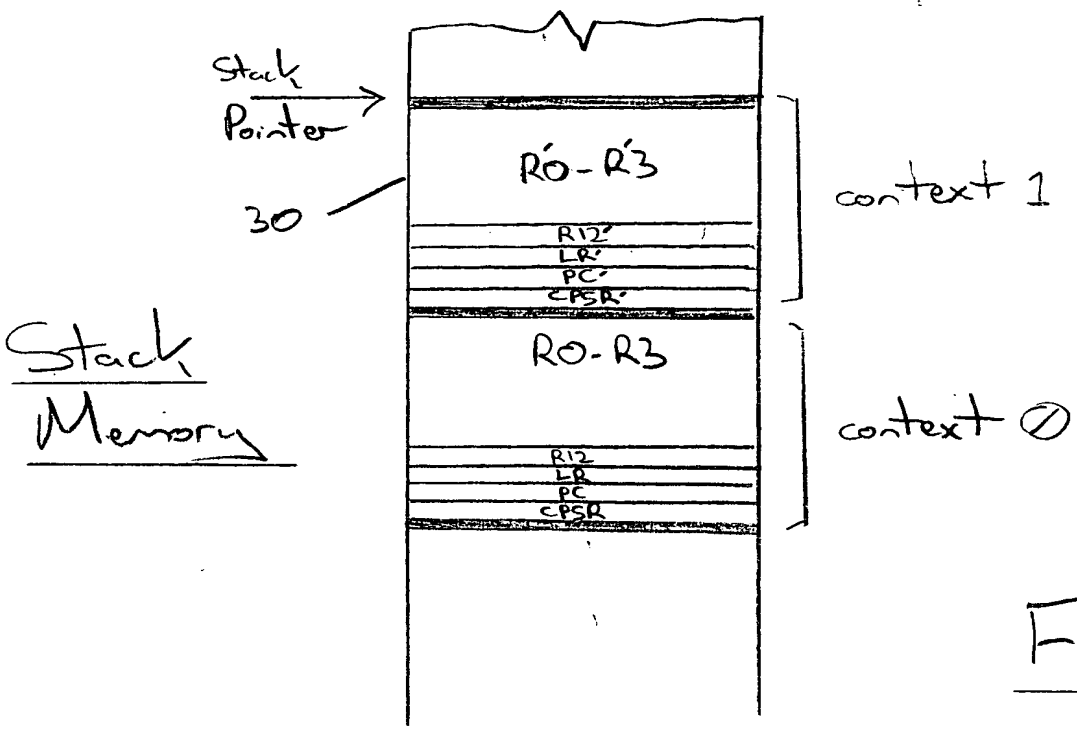

Fig. 3

Priority Inversions

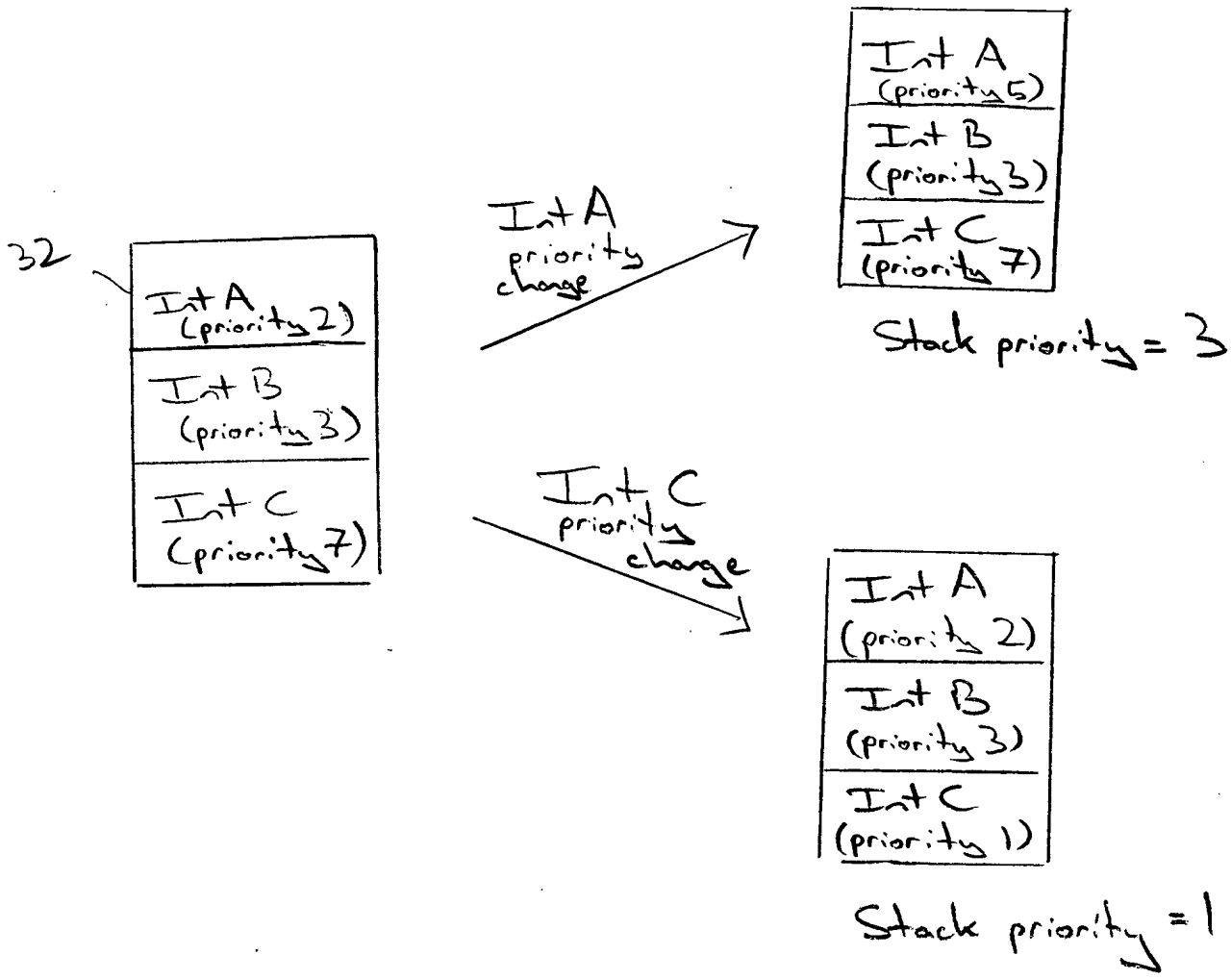

Fig. 4

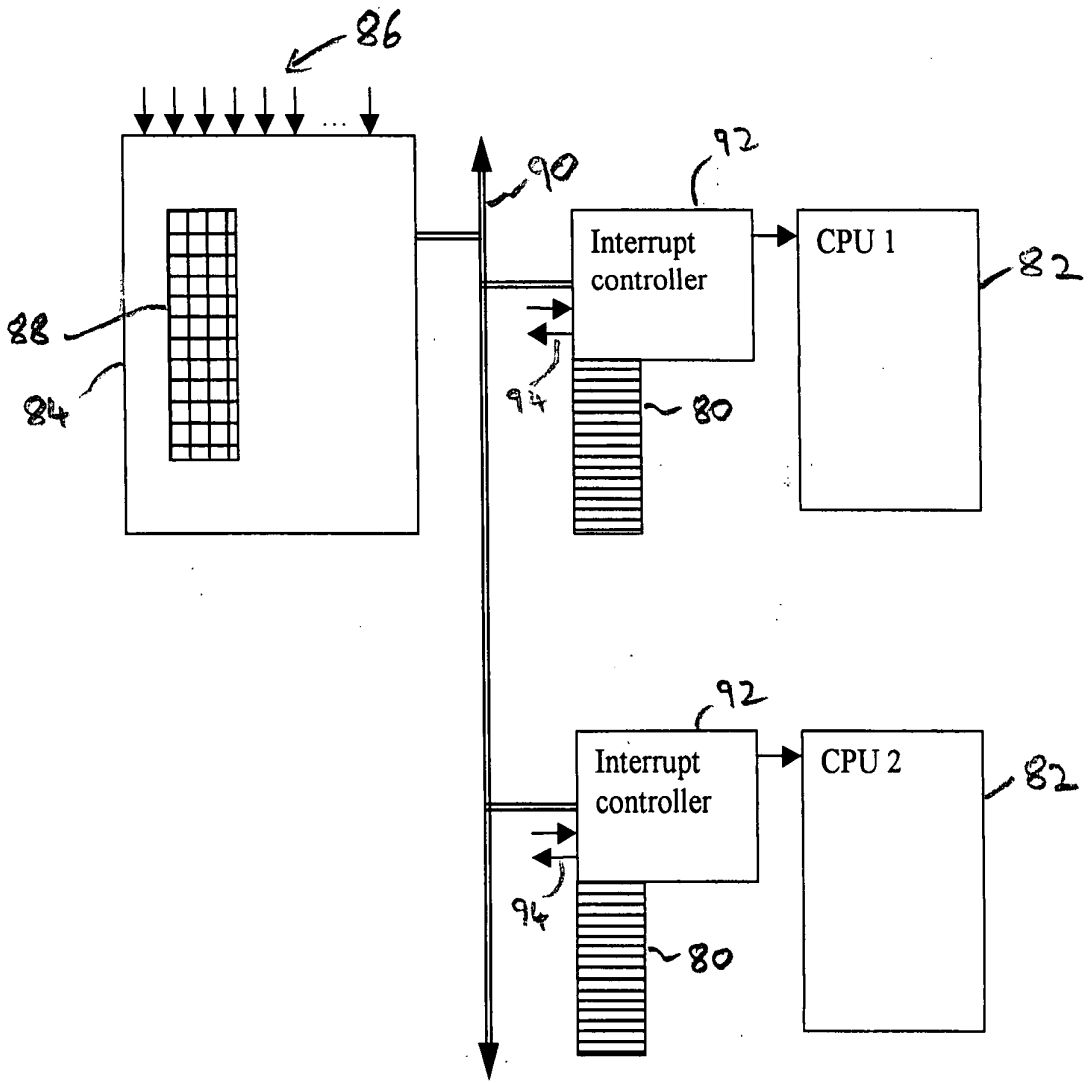
86
90
92
Interrupt controller
CPU 1
82
88
84
94
80
92
Interrupt controller
CPU 2
82
94
80

Fig. 5

Main Flow

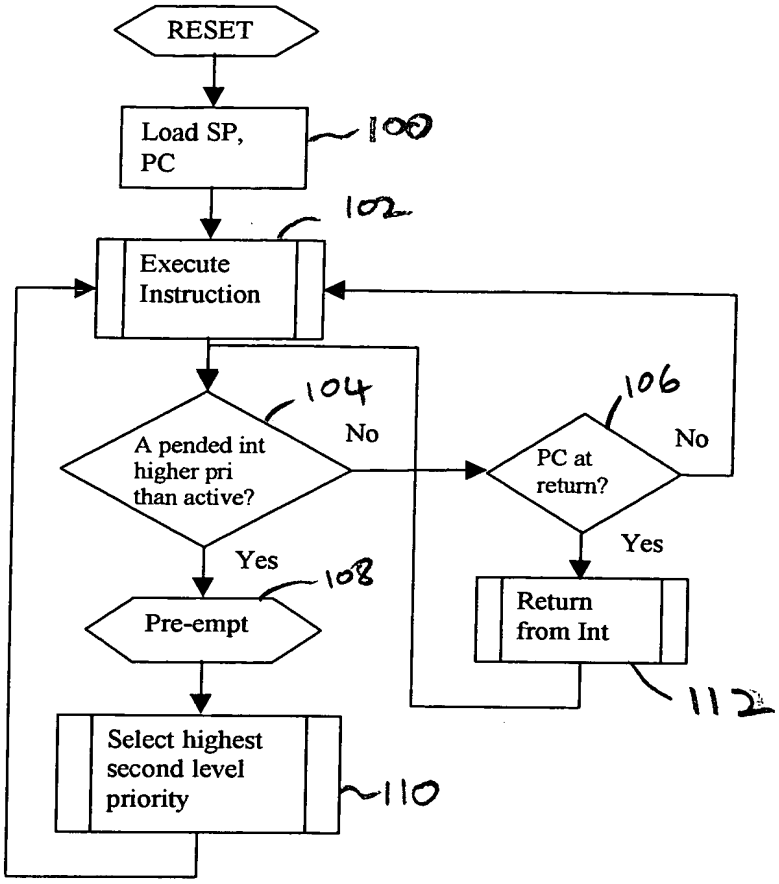

Fig. 6

Main Flow with Tail Chaining

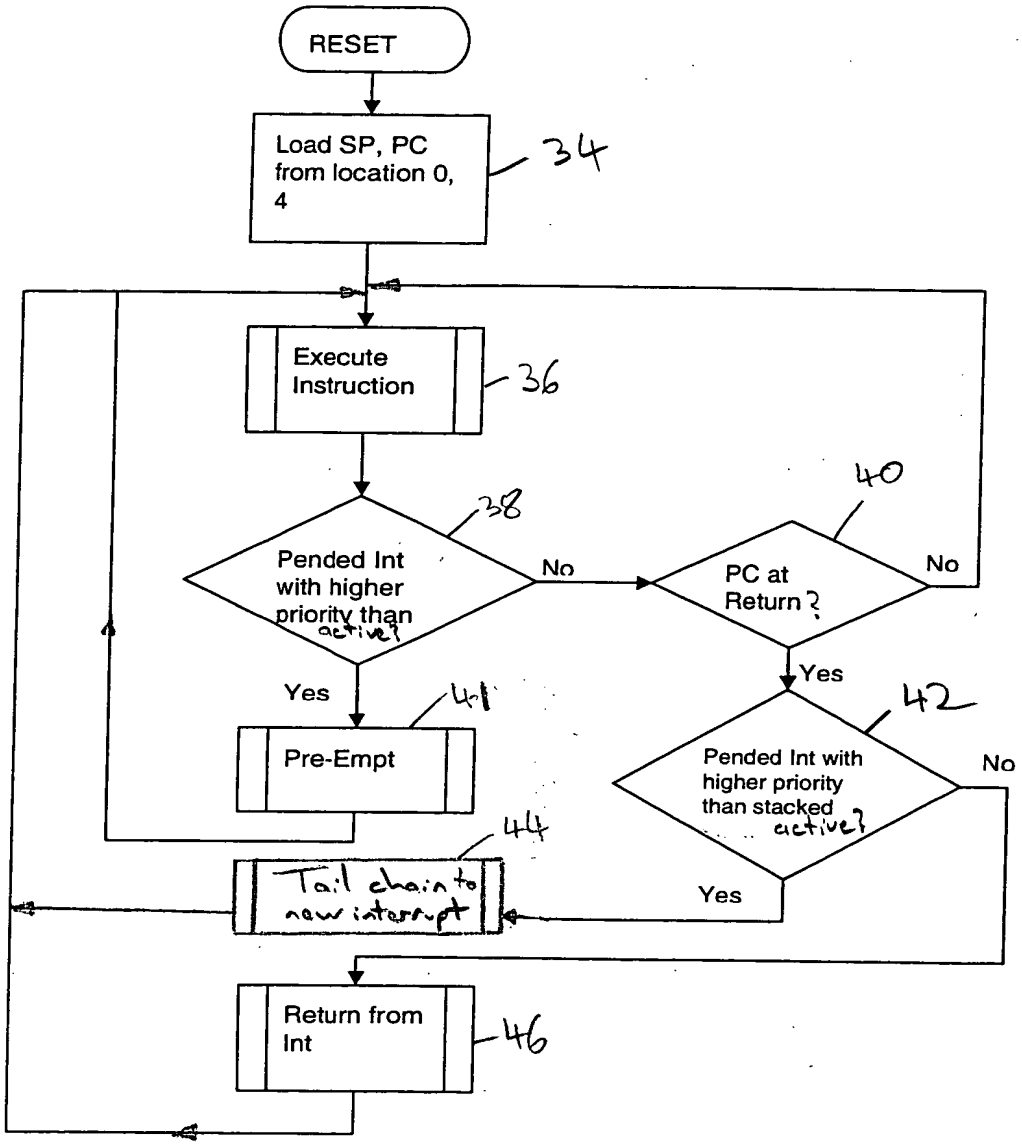

Fig. 7

Pre-emption Flow

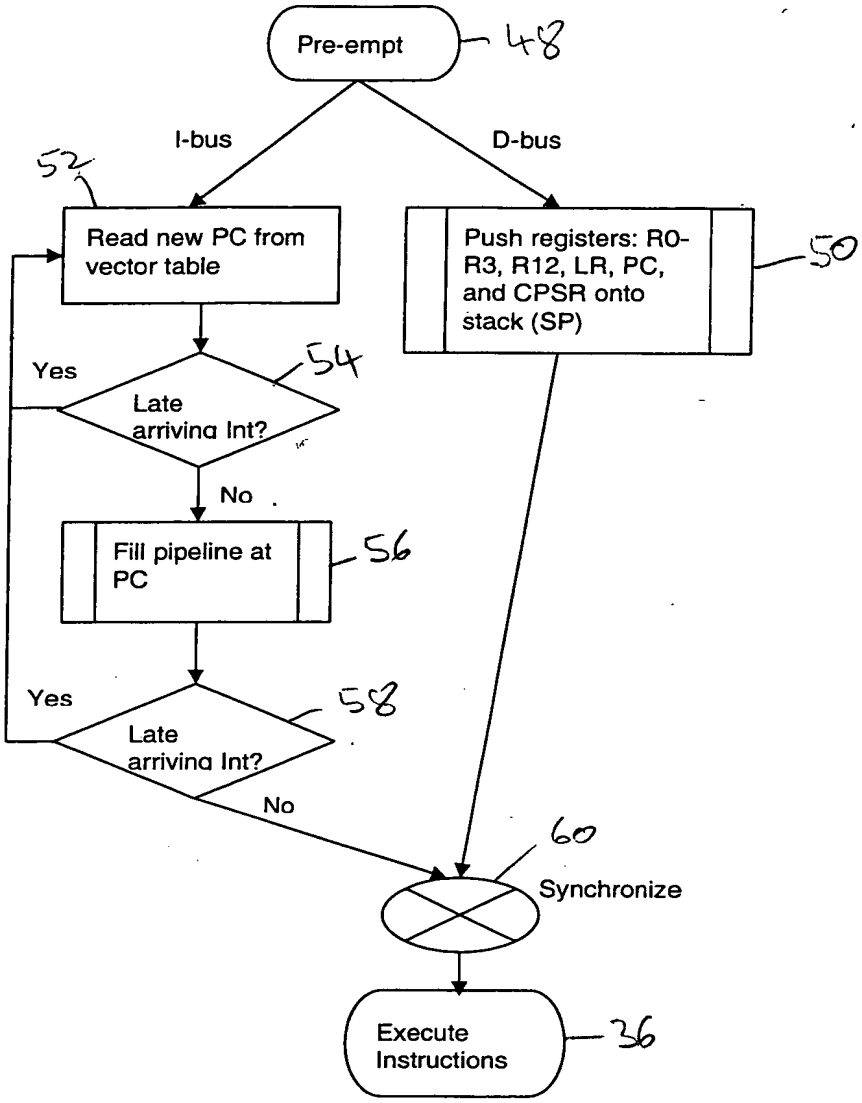

Fig. 8

Return from Interrupt Flow

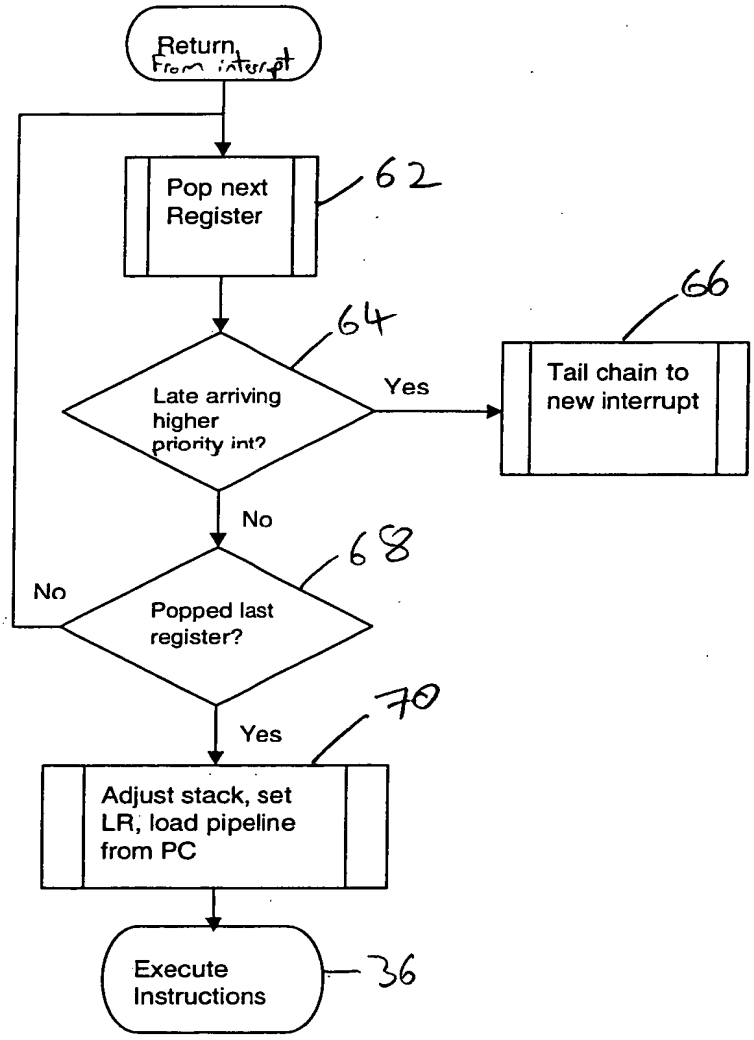

Fig. 9

Tail Chaining Flow

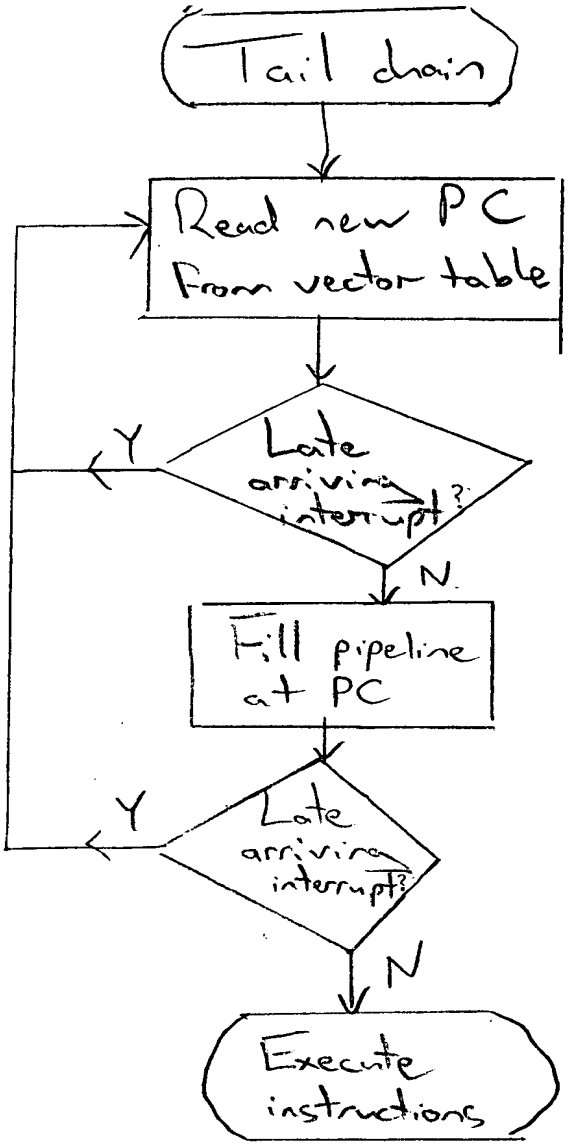

Fig. 10